**In the Claims:**

**A. Kindly cancel Claims 1-5, without prejudice.**

**B. Kindly amend Claims 14-21, as follows.**

14. **(Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising a stacked layer arrangement, and

said stacked layer arrangement comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions; and

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations, said anti-reflective coating material comprising silicon germanium (SiGe).

15. **(Amended)** A semiconductor memory device, as recited in Claim 14,

wherein said anti-reflective coating material further comprises a material selected from a group consisting of silicon oxynitride (SiON) and silicon nitride ($Si_3N_4$), and

wherein said group is compatible with ion implantation and salicidation fabrication processes.

16. **(Amended)** A semiconductor memory device, as recited in Claim 15, wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) and also comprises a pattern formation structure for said at least one peripheral memory element.

17. **(Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising a stacked layer arrangement, and

said stacked layer arrangement comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions; and

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations, wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) and also comprises a pattern formation structure for said at least one peripheral memory element.

18. **(Amended)** A semiconductor memory device, as recited in Claim 17,

wherein said anti-reflective coating material comprises a material selected from a group consisting of silicon oxynitride (SiON), silicon nitride ($Si_3N_4$), and silicon germanium (SiGe), and

wherein said group is compatible with ion implantation and salicidation fabrication processes.

19. **(Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising a stacked layer arrangement, and

said stacked layer arrangement comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions; and

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations,

wherein said anti-reflective coating material comprises silicon germanium (SiGe) being compatible with ion implantation and salicidation fabrication processes, and

wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) and also comprises a pattern formation structure for said at least one peripheral memory element.

20. **(Amended)** A semiconductor memory device, as recited in Claim 19,

wherein said anti-reflective coating material further comprises a material selected from a group consisting of silicon oxynitride (SiON) and silicon nitride ($Si_3N_4$), and

wherein said group is compatible with ion implantation and salicidation fabrication processes.

21. **(Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising a stacked layer arrangement, and

said stacked layer arrangement comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions; and

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said stacked layer arrangement during etching operations,

wherein said anti-reflective coating material comprises a material selected from a group consisting of silicon oxynitride (SiON), silicon nitride ($Si_3N_4$), and silicon germanium (SiGe), said group being compatible with ion implantation and salicidation fabrication processes, and

wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) and also comprises a pattern formation structure for said at least one peripheral memory element.